FPGA-Based Multi-Phase Digital Pulse Width Modulator with Dual-Edge Modulation

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***Abstract*—This paper proposes a new FPGA-based architecture for a multi-phase digital pulse width modulator (MP-DPWM). A novel fine-leading/coarse-trailing edge modulation is applied to allow the sharing of a single fine resolution block for all phases. Specifically, the architecture takes advantage of Digital Clock Manager (DCM) blocks available in modern FPGAs to produce four clock phases from a single clock input to increase the resolution by two bit. An optimized counter/shift-register block is detailed which reduces the size and increases the maximum clock frequency of the architecture for certain numbers of phases. The design was successfully implemented on a low-cost Xilinx Spartan-3 FPGA 9-bit resolution with a switching frequency of 1 MHz and 2–16 phases.**

I. Introduction

In recent years an increasing research interest in digital control of switching mode power supplies (SMPS) is clearly evident [1, 2]. A key reason for this is that digital control has a number of advantages over analog control: such as programmability, reduced sensitivity to external influences, the use of adaptive or other advanced control algorithms along with simpler implementation and prototyping.

A digital controller uses a digital pulse width modulator (DPWM) to generate the control signals for the power supply switches. A sufficiently high resolution of the DPWM is critical for the stability of the output voltage. Conversely, a DPWM resolution that is lower than an ADC resolution leads to limit cycling [3, 4]. To avoid high clock frequencies (i.e. $2^{\#\text{Bit Resolution}} \times f_{\text{switching}}$) needed for simple counter-comparator DPWMs, a range of different hybrid architectures have been proposed and implemented in ICs [5–7] and in field programmable gate arrays (FPGAs) [8–14].

FPGAs are widely used by practicing engineers to prototype and validate their designs. FPGA implementations of digital systems allow for easy and fast prototyping without or before an implementation as an application specific integrated circuit (ASIC).

Modern high-current switched mode power supplies use multiple inductors which are driven in phases in order to split the inductor current and to increase the control loop performance and efficiency. Each phase requires its own DPWM driver signal. This signals are generated by a multi-phase digital pulse width modulator (MP-DPWM), also referred to as digital multiphase modulators (MPM). Different architectures have been proposed in the literature which either require the replication of timing blocks for each phase [15–18] or share the fine resolution block between the phases [19–22].

Furthermore, some multi-phase architectures only support a single common duty cycle for all phases. This limits the controller performance and only permits passive current sharing. Other architectures support independent duty cycles for each phase. This allows the update of the duty cycle with a rate of $P \cdot f_{\text{sw}}$ instead of f_{sw} where P is the number of phases and f_{sw} is the switching frequency. Also variances in the power supply inductors can be compensated by adjusting the duty cycle for the corresponding phases accordingly.

In this paper a new FPGA-based architecture for multi-phase digital pulse width modulators supporting separate duty-cycles for each phase is proposed. It allows the sharing of the fine resolution block across all phases to reduce the implementation size. The architecture is explained in detail, followed by its implementation and verification on an FPGA.

II. Proposed Multi-Phase DPWM Architecture

The proposed architecture is shown in Fig. 1. The course resolution N_c is achieved by a trailing-edge counter/comparator style DPWM stage. A synchronous fine resolution block detailed in [10] for a single-phase trailing-edge DPWM is adapted to support leading-edge modulation. This block increases the DPWM resolution (N) by two bit and requires four out-of-phase clock signals ($0°, 90°, 180°, 270°$) which are produced using dedicated digital clock managers (DCM) available in modern FPGAs. These PLL-type blocks can multiple the frequency and shift the phase of existing clock signals. The rest of the architecture is clocked by the 0° clock.

A. Counter/Comparator Block

This block contains a single counter with $N_{\text{C}} = N - 2$ bit which is shared across all phases. An array of N_{C}-bit adders subtracts the phase difference of each phase from the counter value. The resulting values, “phase values”, drive two arrays of comparators. With reference to Fig. 1, each comparator in the top array tests if the corresponding phase value is all-ones. This indicates that the value will be zero after the next clock edge. Their output signals are named “counter full”. Because some parts of the DPWM need to be triggered when any of the phase values is all-ones, these signals are or-ed together into a single signal name “any counter full”.

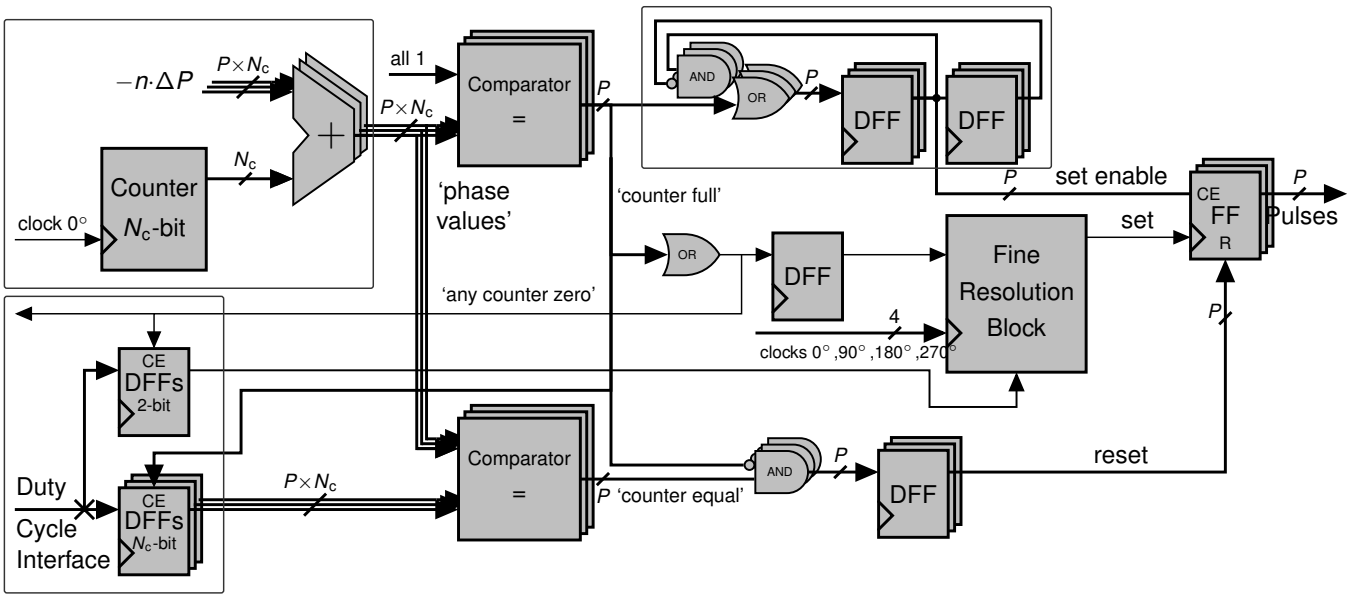


Fig. 1: Schematic of proposed DPWM Architecture.

The comparators in the bottom array test if the corresponding phase value is equal to the most significant N_{C} bit of the duty cycle of this phase. Their output signals are named "counter-equal".

B. Duty Cycle Interface

The duty cycle values arrive from a DPWM-external source, e.g. a PID controller, and are registered one clock cycle before the begin of the switching period by using the "counter full" signals as clock-enable. The duty cycle interface shown in the lower left corner of Fig. 1 uses a single serial N_c-bit wire to receive all duty cycles. The duty cycle of the next phase must be written on this wire and held until it is registered. The lower two LSBs are only needed by the fine resolution block for a few clock cycles directly after they are registered. Therefore a single 2-bit register can be shared by all phases which is controlled by the "any counter full" signal. This signal is also provided to the external block as handshake signal which indicates that the current duty cycle was registered and it is safe to write the next one onto the bus. The "counter full" signals can also be provided to indicate which phase was processed.

If required by the surrounding system a different interface can be used. Alternatively a parallel interface which provides each duty cycle on an N_c-bit wire or a chip-internal bus like AMBA APB which allows addressing of each duty cycle input register separately. To support such interfaces only the two LSB registers must be changed. They cannot be shared and therefore a P-to-1 multiplexer (MUX) is needed to supply the current phase LSBs to the fine resolution block. This MUX uses the "counter full" signals as an one-hot select signal.

C. Output Pulse Registers

The DPWM pulses are produced using D-Flip-Flops (DFFs) due to the absence of Set/Reset-FFs in FPGAs. The output signal of the fine resolution block drives the clock inputs of all pulse DFFs and acts as a shared 'set' signal. The clock enable (CE) inputs of the DFFs are used only to set the pulse register of the current phase. In order to avoid setup and hold time violations of the pulse register, these enable signals must be active one clock cycle before any possible 'set' signal and stay active during the following clock cycle. This is achieved by registering and extending the corresponding "counter-full" signals using the circuit shown in Fig. 2. Because a simple circuit as 2(a) could produce a glitch at the clock transition the circuit 2(b) is proposed which produces a stable, registered clock-enable signals.

The pulse registers are reset by feeding the registered version of the corresponding "counter-equal" signal to their asynchronous reset input. This makes the reset effectively synchronous to the 0° clock.

For very high duty cycles (i.e. the last four fine resolution steps, $D = \{2^N-4, 2^N-1\}$), the reset signal will overlap with the set signal of the next switching cycle. Therefore to counteract this, the reset signal is disabled by an AND gate when the "counter-full" signal is high. The resulting early saturation to 100% duty cycle has no practical influence for use in power supplies.

D. Leading-Edge Fine Resolution Block

The proposed synchronous fine resolution block (FRB) for leading-edge modulation is an adaption of the FRB detailed in [10]. Signal timing and a schematic for this block are shown in Fig. 3 and Fig. 4 respectively. The proposed block contains four DFFs and a 4-to-1 multiplexer (MUX). A pulse generated by a DFF outside the block is used as an input for the four DFFs. This input pulse is produced in the last clock cycle before the start of the next switching period and acts as a timing reference. Each DFF is clocked using one of the

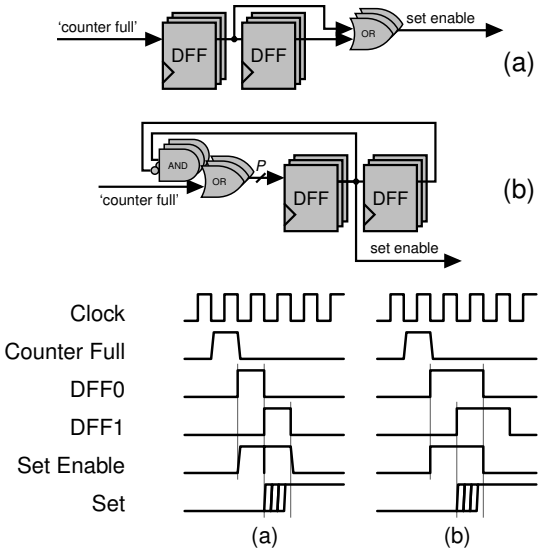


Fig. 2: Schematic and timing diagram of `set enable` logic: (a) simple circuit with potential glitch, (b) proposed glitch-free circuit.

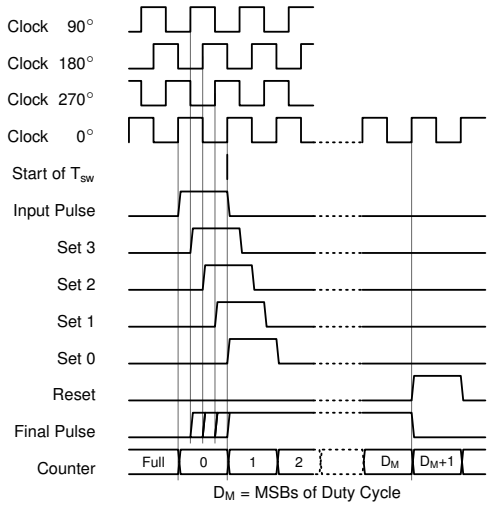


Fig. 3: Timing diagram showing fine leading and coarse trailing pulse modulation.

four clock phases 0°(≙360°), 270°, 180°, 90° and therefore delays the input pulse by a full, ¾, ½ and ¼ clock period, respectively. The DFF outputs are then multiplexed using the two LSBs of the duty cycle as a select signal.

If the duty cycle LSBs are both zero (b00), the full cycle delayed pulse (0° clock) is selected and the block output signal goes high at the start of the switching period. If the LSBs are b01 (=1), b10 (=2) or b11 (=3), the leading edge of the output pulse starts 1, 2 or 3 quarters of a clock cycle earlier, resulting in a longer DPWM pulse.

With the move of the fine-resolution modulation from the trailing to the leading edge, it can be ensured that only one fine-resolution modulation is required at the same time. This

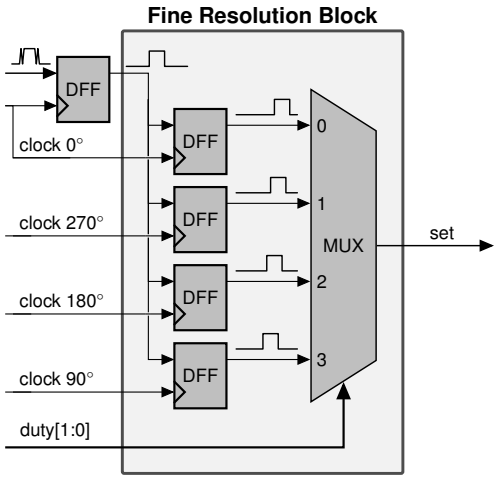


Fig. 4: Schematic of Fine Resolution Block.

allows the sharing of one single fine-resolution block among all phases. Note that if coarse and fine-resolution would be performed at the same edge, such time multiplexing would not be possible, as two different phases might require a fine-resolution modulation at the same time.

E. Counter/Shift-Register Block

This paper also proposes a new counter/shift-register block which can replace the larger counter and all adders (Fig. 5a), leading to a smaller circuit size and to a larger maximal clock frequency due to a reduced logic path. The proposed block can be applied when the number of phases is a power of two. The block consists of a $(N_\mathrm{C} - N_\mathrm{p})$ bit counter and a N_p-bit, $P/2$-stage shift-register, where P is the number of phases and $N_\mathrm{p} = \log_2 P$. The counter holds the common LSBs which are identical for all phases as long as $P = 2^n$. The stages of the shift-register represent the phase-specific MSBs and are loaded, i.e. reset, with the phase-differences at start-up avoiding the requirement of any adders (Fig. 5b).

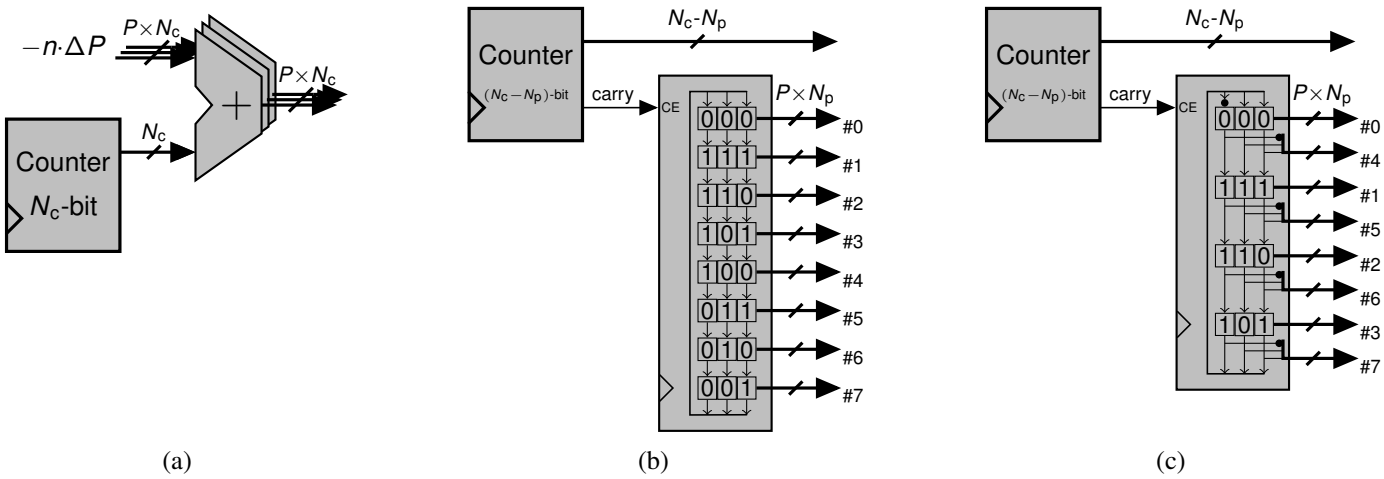
The cyclic shift-register is clocked every time the counter is full. The required control signal can be reused for one of the comparators and therefore does not require additional logic gates. The number of required shift-register stages is reduced from P to $P/2$ by utilizing the symmetry of binary numbers. The values of a phase n and a phase $n + P/2$ differ only by the MSB while the other $N_\mathrm{P} - 1$ bit are identical. The last $P/2$ stages can therefore be replaced by the values of the first $P/2$ stages where the MSB is inverted (Fig. 5c).

III. Experimental Verification

The FPGA implementation of the proposed architecture has been verified by simulation and lab measurements.

A. Implementation

The proposed architecture has been implemented using the hardware description language Verilog. A behaviour/RTL-level coding style has been used to make the implementation vendor independent. The only exception is the clock generating



(a) (b) (c)

Fig. 5: General Counter/Adders Block (a) versus non-optimized (b) and optimized Counter/Shift-Register Block (c) (shown for $P = 8$, $N_\mathrm{p} = 3$).

module (DCM) which must be instantiated using a vendor specific template. However, this module can be encapsulated in an abstract Verilog module which itself instantiates the corresponding clock generator of the used vendor.

A low-cost Xilinx Spartan-3 FPGA has been chosen to verify the architecture. This FPGA provides four DCMs where only one is needed to produce the required four phases of the clock. Additional DCMs can be used to multiply an external clock source to the required clock frequency. For a switching frequency of $f_\mathrm{sw} = 1\,\mathrm{MHz}$, the on-board clock of 50 MHz has been multiplied in two steps to 128 MHz, that is required for a DPWM with 9-bit ($2^{9-2} = 128$) resolution. This results in the use of three DCMs blocks, leaving one for additional tasks. If needed this number can be reduced by matching the different clock frequencies to a common divider. This can be done either by applying an external clock oscillator with a more suitable clock frequency, e.g. 64 MHz, or by using a clock frequency which is a multiple of the FPGA clock, e.g. 100 MHz, which would lead to an odd switching frequency, e.g. $100\,\mathrm{MHz}/2^{9-2} = 0.781\,\mathrm{MHz}$.

B. Simulation Results

The implemented Verilog code has been first simulated using a behavioural simulation model also written in Verilog HDL to verify the correct functional behaviour of the circuit. The synchronous nature of the fine resolution block simplifies this step. Attention must be paid to the correct timing of the comparator and phase enable signals to ensure proper multi-phase operation.

A subsequent post-synthesis gate-level simulation has been performed to include the effect of logic and routing delays into account. Routing delays in the used Spartan-3 FPGA can be around 1ns which is in the range of one LSB (≈2ns). Largely different routing delays in critical paths – between the four DFFs and the MUX of the FRB – can lead to non-linear, even non-monotonic behaviour. For this reason manual placing of the components of the FRB and at least the final output FFs is strongly recommended. The implementation techniques proposed in [10] have been applied to ensure monotony and reduce the offset and non-linearity error. This has been verified by the post-synthesis simulation results.

C. Synthesis Results

The proposed architecture can be implemented by using only a small number of DFFs and Look-Up Tables (LUTs), while the exact size depends on the resolution, the number of phases and the synthesis constraints. A fixed number of DCMs are required as mentioned earlier. An additional Input/Output Block (IOB) which contains the pulse register is required for every phase. The synthesis results for a Xilinx Spartan-3 FPGA (speed grade 4) are shown in Table I. The area results are accurate for all FPGAs with 4-input LUTs. Higher frequencies can be achieved with faster FPGAs, e.g. Xilinx Virtex.

D. Measurement Results

The output pulses of a 16-phase DPWM implemented on a Xilinx Spartan-3 FPGA have been measured and are shown in Fig. 6. The switching frequency is 1 MHz. Fig. 6a displays

TABLE I: Number of Phases vs. Area and Speed

# Phases	FFs	LUTs	Max. f [MHz]
2	24	29	148.7
4	47	41	147.5
8	95	66	148.2
10	131	88	147.2
12	161	105	142.7
14	189	122	138.6
16	215	138	136.4
Pulse Register		P	IOBs
Clock Generation		$1\ldots3$	DCMs
Clock Buffers		$5\ldots7$	GBUFs

the coarse trailing-edge modulation by superposition of three pulses with duty cycles of 6.25% ($^1/_{16}$), 25% and 37.5%. The plot also shows the phase difference of T_{sw}/P between the pulses. The leading-edge modulation of the synchronous fine resolution block is shown in Fig. 6b. It compares the four possible fine steps together with the internal reference input pulse of the fine resolution block. This verifies the pulse timing shown in Fig. 3.

The achieved linearity is shown in Fig. 7. The behaviour is strictly monotonic. The absolute error, i.e. the difference between the ideal and measured pulse width, is around 0.1 LSB (≈200ps). This error is far below the critical level of a 0.5 LSB which allows the implemented DPWM to fully use its 9-bit resolution effectively. The fine resolution block was manually placed as described by [10] to reduce the routing delay differences and to correct the offset error.

IV. Conclusions

In this paper an architecture suitable for implementation of high-speed, high-resolution multi-phase DPWM with high linearity on low-cost FPGAs has been proposed. It supports different duty cycles for every phase to allow active current sharing. The outlined dual-edge modulation allows sharing of the fine resolution block between all phases without the risk of sharing violations. The achieved linearity is approximately 0.1 LSB. The architecture has been implemented and verified on a Xilinx Spartan-3 FPGA with 9-bit resolution and up to 16 phases operating at a switching frequency of 1 MHz.

V. Acknowledgment

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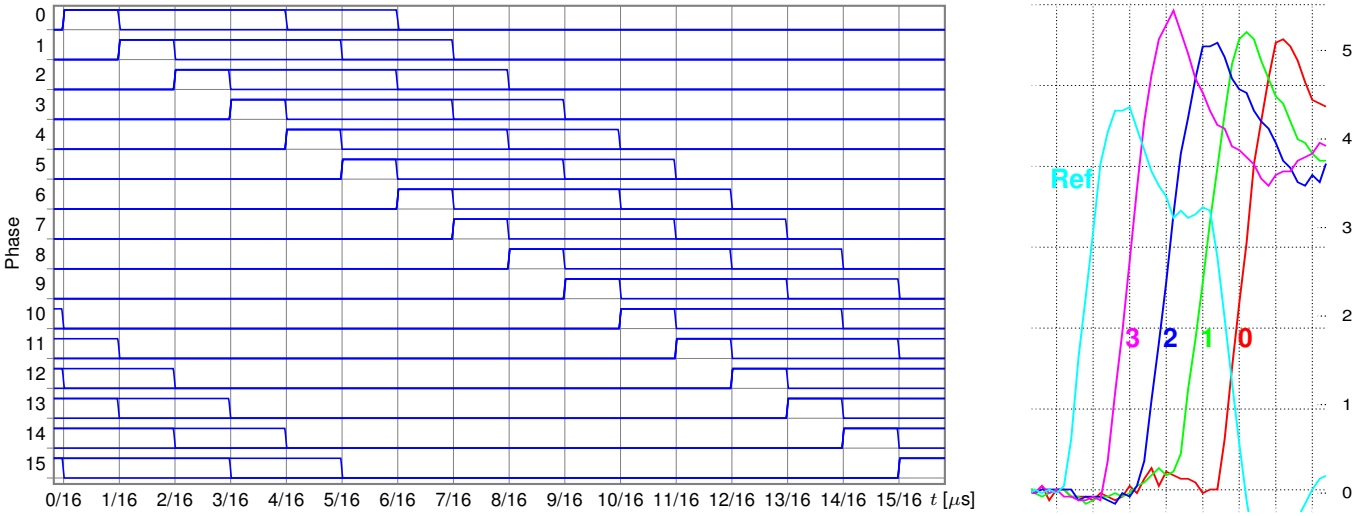

(a) Superposition of $D = \{6.25\%, 25\%, 37.5\%\}$. $[P = 16,\ f_{\text{sw}} = 1\,\text{MHz}]$

(b) Leading-Edge Fine Resolution. [2 ns/div]

Fig. 6: Measured Multi-Phase DPWM Pulses.

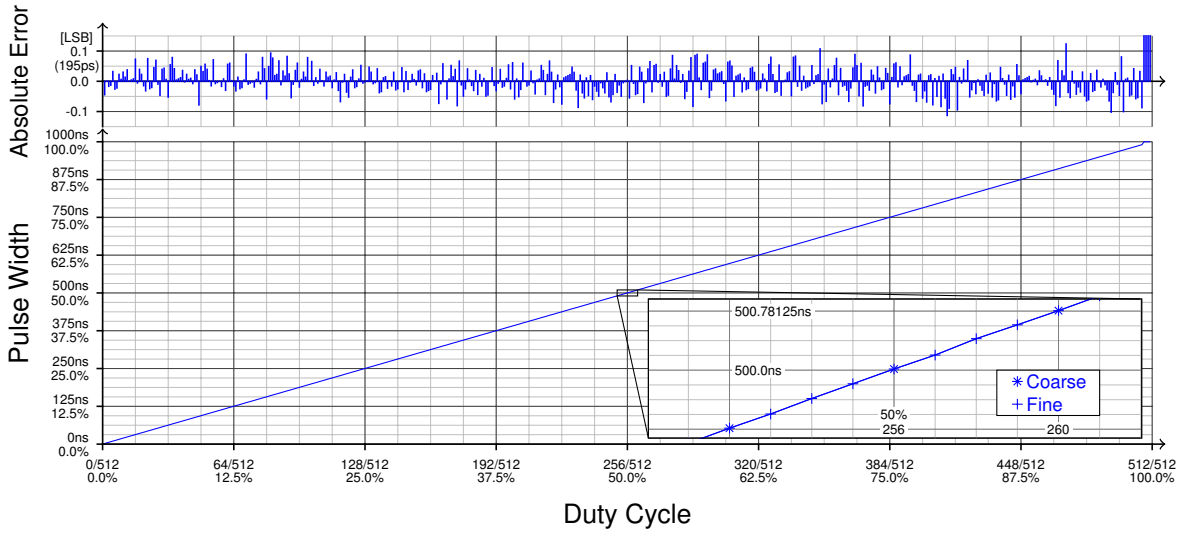

Fig. 7: Measured Linearity of DPWM Pulses